Source region **21** and drift layer **83** are formed to extend to the proximity of a portion immediately beneath finger **45** of gate electrode **42**.

Also in MOSFET **81** having the configuration above, base **44** of gate wiring **43** is arranged between base **24** of source wiring **23** and drain wiring **33**, and base **44** of gate wiring **43** and fingers **25** of source wiring **23** intersect with each other. For this reason, as in RESURF-JFET **1** of the first embodiment, a time lag in gate voltage change is smaller, and time required for charging/discharging a gate circuit is shortened, and therefore, an improved switching speed of MOSFET **81** can be achieved. Furthermore, occurrence of an operationally defective transistor product can be suppressed.

A method for manufacturing MOSFET **81** shown in FIG. **12** is basically the same as the method for manufacturing RESURF-JFET **1** of the first embodiment basically shown in FIG. **8**, however, different in the step of forming drift layer **83** and the step of forming gate electrode **42**. Specifically, steps (S **10**) to (S**20**) shown in FIG. **8** are carried out. Subsequently, on buffer layer **11**, body layer **82** is formed (S**30**). Body layer **82** may have a thickness of 0.6 μm, for example.

At surface **82***a* of body layer **82**, source region **21** and drain region **31** which include a second conductivity type (n type) impurity are then formed (S**60**). This is followed by forming, at surface **82***a* of body layer **82**, drift layer **83** including a second conductivity type (n type) impurity. Subsequently, activation annealing for activating ions implanted into drift layer **83**, source region **21** and drain region **31** is performed (S**70**). Surface **82***a* of body layer **82** is then thermally oxidized to form field oxide film **20** (S**80**).

Openings are then formed in predetermined regions of field oxide film **20** corresponding to positions where source electrode **22** and drain electrode **32** are to be formed in a subsequent step (S**90**). This is followed by forming ohmic electrodes within the openings and simultaneously forming an ohmic electrode corresponding to gate electrode **42** also on field oxide film **20** (S**100**). In this way, source electrode **22** in contact with source region **21**, drain electrode **32** in contact with drain region **31**, and gate electrode **42** on field oxide film **20** are formed. Subsequently, steps (S**110**) to (S**150**) are performed. In this way, MOSFET **81** shown in FIG. **12** can be obtained.

Sixth Embodiment

FIG. **13** is a cross-sectional view of a lateral field-effect transistor of a sixth embodiment. The lateral MESFET (MEtal-Semiconductor Field Effect Transistor) **91** shown in FIG. **13** to serve as an example of the lateral field-effect transistor has the same basic configuration as that of RESURF-JFET **1** of the first embodiment. MESFET **91** is, however, different from RESURF-JFET **1** in having a structure in which Schottky junction gate electrode **42** is formed on channel layer **12** of the semiconductor.

Specifically, in MESFET **91** shown in FIG. **13**, active layer **14** includes p− type buffer layer **11** formed on substrate **10** and n type channel layer **12** formed on buffer layer **11**. Channel layer **12** has surface **12***a*. From surface **12***a* of channel layer **12** to the interior of channel layer **12**, n+ type source region **21** and n+ type drain region **31** are formed. In field oxide film **20** formed on surface **12***a* to serve as an upper surface of channel layer **12**, a plurality of openings are formed.

Within the opening located on source region **21**, source electrode **22** is formed. Source region **21** is formed to oppose finger **25** of source wiring **23**. Source electrode **22** electrically connects finger **25** of source wiring **23** and source region **21**.

Within the opening located on drain region **31**, drain electrode **32** is formed. Drain region **31** is formed to oppose finger **35** of drain wiring **33**. Drain electrode **32** electrically connects finger **35** of drain wiring **33** and drain region **31**.

An opening is also formed in field oxide film **20** between source electrode **22** and drain electrode **32**, and within this opening, gate electrode **42** is formed. Gate electrode **42** is formed below part of finger **45** of gate wiring **43**. Below gate electrode **42**, no gate region described in the first embodiment exists. Gate electrode **42** is directly arranged on surface **12***a* of channel layer **12** and formed to be in contact with channel layer **12** and to exhibit the Schottky characteristics.

Also in MESFET **91** having the configuration above, base **44** of gate wiring **43** is arranged between base **24** of source wiring **23** and drain wiring **33**, and base **44** of gate wiring **43** and fingers **25** of source wiring **23** intersect with each other. For this reason, as in RESURF-JFET **1** of the first embodiment, a time lag in gate voltage change is smaller, and time required for charging/discharging a gate circuit is shortened, and therefore, an improved switching speed of MESFET **91** can be achieved. Furthermore, occurrence of an operationally defective transistor product can be suppressed.

A method for manufacturing MESFET **91** shown in FIG. **13** is basically the same as the method for manufacturing RESURF-JFET **1** of the first embodiment basically shown in FIG. **8**, however, different in that step (S**40**) of forming RESURF layer **13** and step (S**50**) of forming gate region **41** are not performed. Specifically, steps (S**10**) to (S**30**) shown in FIG. **8** are performed. This is followed by forming, at surface **12***a* of channel layer **12**, source region **21** and drain region **31** which include a second conductivity type (n type) impurity (S**60**).

Activation annealing for activating ions implanted into source region **21** and drain region **31** is then performed (S**70**). Surface **12***a* of channel layer **12** is then thermally oxidized to form field oxide film **20** (S**80**). Subsequently, steps (S**90**) to (S**150**) are performed. In this way, MESFET **91** shown in FIG. **13** can be obtained.

It is noted that in describing the first to sixth embodiments, descriptions are given of examples of a lateral field-effect transistor where p type is a first conductivity type and n type is a second conductivity type, however, as to the conductivity type of each component of the lateral field-effect transistor, p type and n type may all be reversed.

Though embodiments according to the present invention have been described above, it should be understood that the embodiments disclosed herein are illustrative and non-restrictive in every respect. The scope of the present invention is defined by the terms of the claims, not by the above description, and is intended to include any modifications within the scope and meaning equivalent to the terms of the claims.

REFERENCE SIGNS LIST

1 RESURF-JFET; **10** substrate; **11** buffer layer; **12** channel layer; **12***a*, **13***a*, **82***a* surface; **13** RESURF layer; **14** active layer; **20** field oxide film; **21** source region; **22** source electrode; **23** source wiring; **24**, **34**, **44** base; **25**, **35**, **45** finger; **31** drain region; **32** drain electrode; **33** drain wiring; **41** gate region; **42** gate electrode; **43** gate wiring; **46** tip; **47** connection; **49** gate pad; **51** interlayer insulating film; **52** passivation film; **61** base region; **62** base electrode; **82** body layer; **83** drift layer; **101** first wiring; **102** second wiring.

The invention claimed is:

1. A field effect transistor comprising:

a substrate;

an active layer formed on said substrate; and